

WHAT IS CLAIMED IS:

- 1 1. A method for performing passive voltage contrast on a silicon on insulator
2 (SOI) device comprising the steps of:
3 grinding a first portion of a substrate of said SOI device with a dimpling tool;
4 etching a second portion of said substrate of said SOI device with
5 tetramethylammonium hydroxide (TMAH) following said grinding of said SOI
6 device with said dimpling tool; and
7 directing a beam of electrons at a backside surface of said SOI device.
- 1 2. The method of claim 1, wherein said beam of electrons is operable for
2 generating a secondary emission of electrons one or more active regions in said SOI
3 device.
- 1 3. The method of claim 2, wherein a presence of said secondary electron
2 emission signals determines a p-type active region, and an absence of secondary
3 emission determines a n-type active region.
- 1 4. The method of claim 2, said secondary emission for inspecting a boundary
2 between a first active region and a second active region of said one or more active
3 regions in said SOI device.
- 1 5. The method of claim 1 further comprising connecting one or more pins of a
2 pin-grid-array package containing said SOI device to a ground reference.
- 1 6. The method of claim 1 further comprising:
2 applying a conductive coating to a topside surface of said SOI device; and
3 connecting said conductive coating to a ground reference.
- 1 7. The method as recited in claim 1, wherein said conductive coating comprises
2 a carbon ink coating.

- 1 8. The method of claim 1 further comprising etching a third portion of said
2 substrate and a portion of a box insulator of said SOI device with hydrofluoric acid
3 (HF) following said etching of said SOI device with said TMAH.

- 1 9. A silicon on insulator (SOI) device, comprising:
2 a substrate;
3 a box insulator overlaying said substrate wherein said box insulator has a
4 backside surface, said backside surface having a portion exposed through said
5 substrate; and
6 a body overlaying said box insulator.
- 1 10. The SOI device as recited in claim 9, further comprising a pin-grid-array
2 package, said SOI device contained in said pin-grid-array package.
- 1 11. The SOI device of claim 9 wherein said portion exposed through said
2 substrate is defined by grinding a portion of said substrate using a dimpling tool and
3 subsequent etching using tetramethylammonium hydroxide (TMAH).
- 1 12. The SOI device of claim 9 wherein a portion of said box insulator is removed.
- 1 13. The SOI device of claim 9 further comprising one or more active regions
2 disposed within said body.
- 1 14. The SOI device of claim 13 further comprising:
2 one or more contacts to corresponding ones of said one or more active
3 regions; and
4 a conductive layer disposed on a topside surface of said SOI device, the
5 conductive layer for interconnecting said one or more contacts to a reference
6 potential.